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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/976,714	10/12/2001	Timothy J. Maloney	42390P11991	2480	
8791	7590 06/05/2003				
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD, SEVENTH FLOOR LOS ANGELES, CA 90025			EXAMINER		
			LAXTON, GARY L		
			ART UNIT	PAPER NUMBER	
			2838		
			DATE MAILED: 06/05/2003		

Please find below and/or attached an Office communication concerning this application or proceeding.

				11					
		cation No.		Applicant(s)					
		76,714		MALONEY ET AL					
Office Action Summa	<i>ry</i> Exam	iner		Art Unit					
	I	L. Laxton		2838					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply									
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status									
1) Responsive to communication	n(s) filed on								
2a) ☐ This action is FINAL .	2b)⊠ This actio	n is non-fir	ıal.						
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.									
Disposition of Claims									
4) Claim(s) 1-20 is/are pending i		idora	tion						
4a) Of the above claim(s)		n considera	ition.						
5) Claim(s) is/are allowed.									
6)⊠ Claim(s) <u>1-19</u> is/are rejected.									
7) Claim(s) <u>20</u> is/are objected to.									
8) Claim(s) are subject to restriction and/or election requirement. Application Papers									
9) The specification is objected to by the Examiner.									
10)⊠ The drawing(s) filed on <u>12 Öctober 2001</u> is/are: a)□ accepted or b)⊠ objected to by the Examiner.									
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).									
11) ☐ The proposed drawing correction filed on is: a) ☐ approved b) ☐ disapproved by the Examiner.									
If approved, corrected drawings are required in reply to this Office action.									
12) The oath or declaration is objected to by the Examiner.									
Priority under 35 U.S.C. §§ 119 and 120									
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).									
a) ☐ All b) ☐ Some * c) ☐ Non									
1. Certified copies of the p	-								
2. Certified copies of the priority documents have been received in Application No									
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 									
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).									
a) ☐ The translation of the foreign language provisional application has been received. 15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.									
Attachment(s)									
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Re 3) Information Disclosure Statement(s) (PTO-1		5) 🔲		(PTO-413) Paper No Patent Application (PT					

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DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the third current sink transistor coupled in series with the first current sink transistor of claim 5; and the voltage divider adapted to provide a second intermediate voltage potential and the second drive circuit comprises an inverter with an input coupled to receive the second intermediate voltage potential of claim 6; a static random access memory and an integrated circuit of claim 9 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

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The specification is silent regarding claims 5 and 6. The examiner is unable to locate any explanation regarding a third current sink transistor coupled in series with the first current sink and a second drive circuit to provide an enabling voltage to the third current sink; and the voltage divider provides a second intermediate voltage potential and a second drive circuit receives the second intermediate voltage.

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The applicant should refrain from using legal phraseology such as in accordance with one embodiment" in the abstract.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

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<u>;</u>;

The applicant generally and broadly recites ESD protection which does not distinguish and is not clearly indicative of the invention to which the claims are directed.

Claim Objections

5. Claim 6 is objected to because of the following informalities: the end of the sentence requires a period. Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 7. Claims 1-6, 9, 18 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Maloney (US 5,956,219).

As to claim 1, an apparatus (figure 4) having an electrostatic discharge (ESD) device (400) comprising: a voltage divider (408, 410) to provide a first intermediate voltage potential (414); a first current sink transistor (404) and a second current sink transistor (402) coupled in series; and a first drive circuit (420, 422) to provide an enabling voltage potential to the second current sink transistor (402), wherein the drive circuit comprises an inverter (420) with an input (441) coupled to receive the first intermediate voltage potential (414).

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As to claim 2, the first current sink transistor and the second current sink transistor are p-channel transistors: figure 4.

As to claims 3, the first current sink transistor and the second current sink transistor are formed in a same well in a semiconductor substrate (col. 3 lines 48-50).

As to claim 5, the ESD device (400) further comprises: a third current sink transistor (406) coupled in series with the first current sink transistor (404); and a second drive circuit (426, 428, 442, 443) to provide an enabling voltage potential to the third current sink transistor (406). As to claim 6, the voltage divider (408, 410) is adapted (412) to provide a second intermediate voltage potential (416) and the second drive circuit (426, 428, 442, 443) comprises an inverter (426) with an input (442, 443) coupled to receive the second intermediate voltage potential (416).

<u>NOTE</u>: "ADAPTED TO": It has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138.

As to claim 9, static random access memory (col. 3 line 33); and an integrated circuit (figure 1, 100), the integrated circuit having an electrostatic protection circuit (figure 5) comprising: a first tier (508, 516, 507, 506) including an RC timer (figure 5, 512, 510) and a first current sink transistor (502); and a second tier (figure 5, 514, 515, 522, 524) wherein the second tier is coupled to the RC timer (at 517 to 512).

As to claim 18, a method of enabling an electrostatic discharge device (figure 3, 300) comprising: enabling a first tier (348, 345, 318, 312, 340, 342, 324) and a second tier (326, 322, 344, 316) of the electrostatic discharge device (300) with an RC timer (348, 345) in the first tier. As to claim 19, providing an intermediate voltage potential (303) to the second tier (@ 326) with a voltage divider (302, 304).

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Claim Rejections - 35 USC § 103

- 8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 10-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maloney (US 5,956,219).

As to claim 7, Maloney discloses the claimed invention as stated above in regards to claim 1 except for wherein the voltage divider comprises at least four transistors coupled in series.

Maloney does disclose, in figure 3, coupling two transistors in series (302, 304) to form a voltage divider. And then in figure 3 Maloney discloses coupling three transistors in series (408, 410, 412) to form a voltage divider with an additional tap in order to provide a second intermediate voltage potential to be used by the circuit.

Therefore, to add a fourth transistor in series with the other three is considered to be merely determining an optimum value and it would have been obvious to one having ordinary skill in the art at the time the invention was made to add a fourth transistor in series with the existing three in order to tap a third potential voltage to be used in the circuit or to add additional voltage divider elements to divide the input voltage to a desired or proper voltage for circuit use since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 167 F.2d 272, 205 USPQ 215 (CCPA 1980).

As to claim 10, further comprising a voltage divider (514, 516) coupled to the first tier and the second tier to provide an intermediate voltage potential (517).

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As to claim 11, wherein the second tier includes an inverter (522, 524) having an input terminal (thru 520) coupled to receive the intermediate voltage potential (517).

As to claims 12-14, wherein the first tier includes an inverter (507, 506) having an input terminal coupled to the RC timer (512 p-channel, 510 capacitor) (figure 5). Claim 14 is given no patentable weight beyond a capacitor connected to an input of the inverter due to "adapted to" claim language.

<u>NOTE</u>: "ADAPTED TO": It has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138.

As to claim 15, Maloney discloses the claimed invention as stated above in regards to claim 9 except for wherein the voltage divider comprises at least four transistors coupled in series.

Maloney does disclose, in figure 3, coupling two transistors in series (302, 304) to form a voltage divider. And then in figure 3 Maloney discloses coupling three transistors in series (408, 410, 412) to form a voltage divider with an additional tap in order to provide a second intermediate voltage potential to be used by the circuit.

Therefore, to add a fourth transistor in series with the other three is considered to be merely determining an optimum value and it would have been obvious to one having ordinary skill in the art at the time the invention was made to add a fourth transistor in series with the existing three in order to tap a third potential voltage to be used in the circuit or to add additional voltage divider elements to divide the input voltage to a desired or proper voltage for circuit use since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 167 F.2d 272, 205 USPQ 215 (CCPA 1980).

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As to claim 17, the voltage divider (514, 516) comprises at least two transistors (514, 516) coupled in series between voltage potential rails (Vcc and ground) (figure 5).

9. Claims 8 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maloney (US 5,956,219) in view of Pilling et al.

As to claim 8, Maloney discloses the claimed invention as stated above in regards to claim 1 except for wherein the ESD device further comprises a latch coupled to the voltage divider; and as to claim 16. Maloney discloses the claimed invention as stated above in regards to claim 9 except for further comprising a latch coupled to the voltage divider.

Pilling et al teaches coupling a latch circuit (118) to a voltage divider (Q2, Q3, Q7) in a circuit for improving the reliability of antifuses by storing the state of an antifuse in a latch and thus is available for continuous sampling without subjecting the antifuse to additional read voltages, since an antifuse coupled to a programming pin and all other antifuses are susceptible to damage from ESD levels unless they are adequately protected from the ESD levels (col. 2 and col.3). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Maloney to add a latch to the voltage divider as taught by Pilling et al in order to couple the latch circuit to a voltage divider to store the state of any particular part of the circuit to be available for sampling at a desired time in order to determine the state of the circuit after sampling.

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Allowable Subject Matter

- 10. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 11. The following is a statement of reasons for the indication of allowable subject matter: prior art of record fails to disclose or suggest, inter alia, an apparatus, wherein providing an intermediate voltage potential includes providing the intermediate voltage potential to an input terminal of an inverter in the second tier.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6,008,970 Maloney et al discloses clamp circuitry for ESD.

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13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (703) 305-7039. The examiner can normally be reached on Monday thru Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (703)308-1680. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-7724 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

MICHAEL SHERRY SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2800